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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,566	03/30/2004	Susanne A. Paul	SIL.P0077	4126

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EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,566	PAUL ET AL.	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08-9-2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant states that "An IDS will be following this amendment" in the response dated 8-9-2005. However, no such response is in the file at the time of this Office Action.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 50-52, 54-56, 58-65, 67-69, 71, 72, 74, 76-80 and 82-84 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 56-59 of copending Application No. 10/812,853. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the '566 and '853 applications uses different terminology to claim the same subject matter and the above indicated claims of the instant '566 application fails to present a patentable distinction over the claims of the '853 application. For example the claims of the '566 recite a first transistor connected to a first supply voltage node and a second transistor coupled to a second supply voltage node, this fails to provide for a patentable distinction over that of the '853 claimed invention for having the first and second transistors coupled between a voltage differential involves the coupling of the first transistor connected to a first supply voltage node and the second transistor coupled to a second supply voltage node. Likewise the additional limitation of having a ground as one of the supply voltage nodes in the '566 application, it is common place to utilize a ground as one of the voltage nodes in an amplifier circuit and as the selection of the value of these voltage supply values is a result effective variable that involves routine skill in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to select ground as one of the voltage supply potentials in the claims invention of the '853 application, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Claims like claim 62 of the '566 application recites that the first

transistor is coupled between the supply voltage and a first output node and also recites a second output node. While the claims of the '853 application are silent on calling the two nodes where the inductance is coupled between the first and second transistors first and second output nodes they most certainly are output nodes as these nodes do output something to the inductor and the inductor outputs to the transistors. The naming of the nodes of the '853 application does not provide for a patentable distinction of the claims of the '566 application over the claims of the '853 application. Also the inductor can be considered "a load is coupled to the first and second output nodes." Although note that the claims between the two applications are not identical in scope, they are not claiming the same invention, it is just that the claims of the instant applicant ('566 application) are unpatentable over the above indicated claims of the '853 application. Claims like 56 of the '566 application recites the additional limitation of having a load coupled to the inductor that is not recited in the '853 application. This fails to provide a patentable distinction over the claimed invention.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claims 47-49, 53, 57, 66, 70, 73, 75, 81 and 85 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 47-66 of copending Application No. 10/812,853 in view of Kawai et al. 5,994,963 (Kawai).

Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the '566 and ''853 applications uses different terminology to claims the same subject matter and the above indicated claims of the instant '566 application fails to present a patentable distinction over the claims of the '853 application. For example the claims of the '566 recite a first transistor connected to a first supply voltage node and a second transistor coupled to a second supply voltage node, this fails to provide for a patentable distinction over that of the '853 claimed invention for having the first and second transistors coupled between a voltage differential involves the coupling of the first transistor connected to a first supply voltage node and the second transistor coupled to a second supply voltage node. Likewise the additional limitation of having a ground as one of the supply voltage nodes in the '566 application, it is common place to utilize a ground as one of the voltage nodes in an amplifier circuit and as the selection of the value of these voltage supply values is a result effective variable that involves routine skill in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to select ground as one of the voltage supply potentials in the claims invention of the '853 application, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215

(CCPA 1980). Applicant is also referred to the reasoning as presented in the double patenting rejection of claims 50-52, 54-56, 58-65, 67-69, 71, 72, 74, 76-80 and 82-84 involving the '853 application as this reasoning applies here especially for the parent claims to claims like 53, etc.. Claims like claim 47 recites the additional limitation of a transformation network coupled between the first and second switching devices and a load.

Figures 7-9 and the relevant text of Kawai discloses a power amplifier arrangement that includes two switching devices like elements 45 and 46 (Note that transistors are well known to be considered switching devices.), a voltage potential is applied across these transistors as is clearly illustrated and an inductor like 67 is coupled between these two switching devices. This is exactly the same switching structure as that claimed in the '853 application. Kawai also teaches a transformation network composed of capacitors like 47 and 68 that is coupled between the first and second switching devices and a load. Capacitance 47 is clearly a high pass filter that passes the AC and blocks DC. Capacitance 68 "causes signals having frequencies lower than the signal to be amplified by the E-type MESFET 45 and noise applied from the drain voltage source via the drain voltage input terminal 44 to flow to ground" (See column 11, around line 26 of Kawai.). Note the output of Kawai is connected to a load although the load is not shown in Figure 7-9.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provided a load coupled to the inductor through a transformation network coupled between the first and second switching devices and a load in the '853 application so as to block DC and filter noise that would be passed to the load otherwise as taught by Kawai.

This is a provisional obviousness-type double patenting rejection.

Claims 50-52, 54-56, 58-65, 67-69, 71, 72, 74, 76-80 and 82-84 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 47-80 of copending Application No. 10/812,858. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the '858 application has all the details of the '566 application except for that noted below. This includes, for example, forming an inductor or inductance between first and second switching devices and thus an inductor is present between the first and second switching devices as recited in the '566 application. It is noted that the '566 application recites structure but this structure is the result of and is part of the method steps of the '858 application. Claims like claim 50 of the '566 application recites first transistor and a second transistor whereas as noted above the '858 application recites a first and second transistor. A transistor is a conventionally known switching device. The addition of this limitation to the claims of the '858 application does not

present a patentable distinction over the claims of the '566 application because it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the generic switching devices of the claimed '858 application with transistors since the examiner takes Official Notice of the equivalence of a transistor and a switching device for there use in the electronic art and the selection of any of these known equivalents to provide a switching function would be within the level of skill in the art. In other words one of ordinary skill in the art would have been motivated to make the substitute because of the art-recognized equivalence. Note that coupling the switching devices between a voltage differential must involve first and second supply voltage nodes. There must be two terminals or nodes for there to be a voltage differential. Also note that the inductance would be considered a load. Likewise the additional limitation of having a ground as one of the supply voltage nodes in the '566 application, it is common place to utilize a ground as one of the voltage nodes in an amplifier circuit and as the selection of the value of these voltage supply values is a result effective variable that involves routine skill in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to select ground as one of the voltage supply potentials in the claims invention of the '858 application, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claims 47-49, 53, 57, 66, 70, 73, 75, 81 and 85 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 47-66 of copending Application No. 10/812,858 in view of Kawai et al. 5,994,963 (Kawai).

Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the '858 application has all the details of the '566 application except for that noted below. This includes, for example, forming an inductor or inductance between first and second switching devices and thus an inductor is present between the first and second switching devices as recited in the '566 application. It is noted that the '566 application recites structure but this structure is the result of and is part of the method steps of the '858 application. Claims like claim 50 of the '566 application recites first transistor and a second transistor whereas as noted above the '858 application recites a first and second transistor. A transistor is a conventionally known switching device. The addition of this limitation to the claims of the '858 application does not present a patentable distinction over the claims of the '566 application because it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the generic switching devices of the claimed '858 application with transistors since the examiner takes Official Notice of the equivalence of a transistor and a switching

device for there use in the electronic art and the selection of any of these known equivalents to provide a switching function would be within the level of skill in the art. In other words one of ordinary skill in the art would have been motivated to make the substitute because of the art-recognized equivalence. Note that coupling the switching devices between a voltage differential must involve first and second supply voltage nodes. There must be two terminals or nodes for there to be a voltage differential. Also note that the inductance would be considered a load. Likewise the additional limitation of having a ground as one of the supply voltage nodes in the '566 application, it is common place to utilize a ground as one of the voltage nodes in an amplifier circuit and as the selection of the value of these voltage supply values is a result effective variable that involves routine skill in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to select ground as one of the voltage supply potentials in the claims invention of the '858 application, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims like claim 47 recites the additional limitation of a transformation network coupled between the first and second switching devices and a load.

Figures 7-9 and the relevant text of Kawai discloses a power amplifier arrangement that includes two switching devices like elements 45 and 46 (Note that transistors are well known to be considered switching devices.), a voltage potential is applied across these transistors as is clearly illustrated and an inductor like 67 is coupled between these two switching devices. This is exactly the same switching structure as that claimed in the '853 application. Kawai also teaches a transformation network composed of capacitors like 47 and 68 that is coupled between the first and second switching devices and a load. Capacitance 47 is clearly a high pass filter that passes the AC and blocks DC. Capacitance 68 "causes signals having frequencies lower than the signal to be amplified by the E-type MESFET 45 and noise applied from the drain voltage source via the drain voltage input terminal 44 to flow to ground" (See column 11, around line 26 of Kawai.). Note the output of Kawai is connected to a load although the load is not shown in Figure 7-9.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provided a load coupled to the inductor through a transformation network coupled between the first and second switching devices and a load in the '858 application so as to block DC and filter noise that would be passed to the load otherwise as taught by Kawai.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 and after July 15, 2005 the fax number will be 571-273-8300. Note that old fax number (703-872-9306) will be service until September 15, 2005.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
October 22, 2005

Michael B Shingleton
Primary Examiner
Group Art Unit 2817